PRODUCT/PROCESS
CHANGE NOTIFICATION

PCN AMS/18/10890

Analog, MEMS & Sensors Group (AMS)

Qualification of ST Bouskoura as Assembly and Test & Finishing site for selected products in SO8 package

General Purpose Analog Division

WHAT:

Progressing on activities related to production rationalization and capacity increase, ST is pleased to announce the transfer of some GPA (General Purpose Analog) products from ST Shenzhen to ST Bouskoura.

Please find more information related to the transfer of the impacted products:

Material	Current process	Modified process	Comment
Diffusion location	No change		No change
Assembly location	ST Shenzhen	ST Bouskoura	
Test location	ST Shenzhen	ST Bouskoura	
Molding compound	Sumitomo G700KC	Sumitomo G700KC	No change
Die attach	ABLESTIK 8601S-25	ABLESTIK 8601S-25	No change
Lead frame	Copper 98x150mils	Copper 94x125mils	Pad size reduction
Wire	Copper wire 1 mil	Copper wire 1 mil	No change
Plating	Preplated e4	Matte Sn (e3)	
MSL	1		No change

Samples of vehicle test are available now and other samples will be launched upon customer's re-quests. Please submit requests for samples within 30 days of this notification.

WHY:

The purpose of the transfer is to rationalize our production tool and increase capacity.

HOW:

•The qualification is based on representative Test vehicles, using internal ST rules for changes.
•To validate the change, dedicated engineering trials have been performed and reliability report is attached.

IMPACTS OF THE CHANGE:

Form/Fit/Fonction : No change

WHEN:

For all impacted products, estimated 1st shipment start date is wk32 2018.

Marking and traceability:

Unless otherwise stated by customer's specific requirement, the traceability of the parts assembled with the new material set will be ensured by new internal sales type, date code and lot number.

The changes here reported will not affect the electrical, dimensional and thermal parameters keeping unchanged all the information reported on the relevant datasheets.
There is -as well- no change in the packing process or in the standard delivery quantities.

Lack of acknowledgement of the PCN within 30 days will constitute acceptance of the change. After acknowledgement, lack of additional response within the 90 day period will constitute acceptance of the change (Jedec Standard No. 46-C).

Shipments may start earlier with the customer's written agreement.

STMicroelectronics

Manufactured under patents or patents pending

Assembled in: COUNTRY
PbFree Second level interconnect
MSL: X Bag sealed date: XX XXX XXXX
PBT: XXX°C Catergory: ECOPACK/Rohs

TYPE Commercial product
Finished good

Total Qty: XXXX

Trace codes PPYWWLLL WX TF
PPYWWLLL WX TF
PPYWWLLL WX TF

Marking **MARKING**

Bulk Id Number

Bar code

Please provide the bulk Id for any inquiry

On trace code "PP" code will move from "GK" (ST Shenzhen) to "CZ" (ST Bouskoura)

Reliability Report

Qualification of ST Bouskoura as Assembly and Test & Finishing site for selected products in SO8 package of GPA Division

General Information	
Product Line	*UW23*
Product Description	3.3 V powered, 15 kV ESD protected, up to 12 Mbps RS-485/ RS-422 transceiver
P/N	ST3485ECDT
Product Group	*AMS*
Product division	*General Purpose Analog &RF*
Package	*SO8*
Silicon Process technology	*BCD3S*

Locations	
Wafer fab	*ST Singapore,*
Assembly plant	*ST Bouskoura*
Reliability Lab	*, ST Catania*

Related products

ST1480ABDR
ST1480ACDR
ST3485EBDR
ST3485ECDR
ST3485EIDT
ST4485EBDR

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
This report does not imply for STMicroelectronics expressly or implicitly any contractual obligations other than as set forth in STMicroelectronics general terms and conditions of Sale. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics.

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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
0061692	Reliability tests and criteria for qualifications

2 GLOSSARY

DUT	Device Under Test
PCB	Printed Circuit Board
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

To qualify the transfer of the ST3485ECDT and related products in SO8 package from ST Shenzhen to ST Bouskoura for General purpose analog.

3.2 Conclusion

Qualification Plan requirements will have to be fulfilled without issue. It is stressed that reliability tests have to show that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests have to demonstrate the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

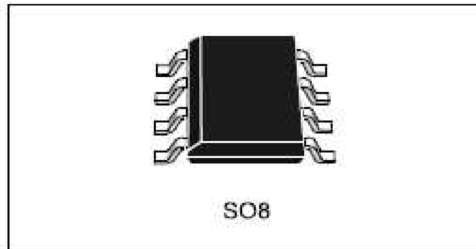
4 DEVICE CHARACTERISTICS

4.1 Device description

ST3485EB, ST3485EC, ST3485EI, ST3485EIY

3.3 V powered, 15 kV ESD protected, up to 12 Mbps RS-485/ RS-422 transceiver

Datasheet - production data



Features

- ESD protection
  - ±15 kV IEC 61000-4-2 air discharge
  - ±8 kV IEC 61000-4-2 contact discharge
- Operate from a single 3.3 V supply - no charge pump required
- Interoperable with 5 V logic
- 1 µA low current shutdown mode max.
- Guaranteed 12 Mbps data rate
- -7 to 12 V common mode input voltage range
- Half duplex versions available
- Industry standard 75176 pinout
- Current limiting and thermal shutdown for driver overload protection
- Guaranteed high receiver output state for floating inputs with no signal present
- Allow up to 64 transceivers on the bus
- Available in SO8 package
- Automotive grade (ST3485EIY)

Description

The ST3485EB/EC/EI/EIY device is ±15 kV ESD protected, 3.3 V low power transceiver for RS-485 and RS-422 communications. The device contains one driver and one receiver in half duplex configuration.

The ST3485E device transmits and receives at a guaranteed data rate of at least 12 Mbps.

All transmitter outputs and receiver inputs are protected to ±15 kV IEC 61000-4-2 air discharge.

The driver is short-circuit current limited and is protected against excessive power dissipation by thermal shutdown circuitry that places the driver outputs into a high impedance state.

Table 1: Device summary

Order code	Temp. range	Package	Packing
ST3485ECDR	0 to 70 °C	SO8 (tape and reel)	2500 parts per reel
ST3485EBDR	-40 to 85 °C		
ST3485EIDT	-40 to 125 °C		
ST3485EIYDT			

4.2 Construction note

	P/N ST3485ECDR	**P/N STM706YM7F**	**P/N LM393DT**
Wafer/Die fab. information			
Wafer fab manufacturing location	ST Singapore	ST Singapore	ST Singapore
Technology	BCD3S	HCMOS4	Bipolar
Die finishing back side	RAW SILICON	RAW SILICON	RAW SILICON
Die size (microns)	1950x2720	1350 x 1510µm	950 x 870 µm
Bond pad metallization layers	AlSi	AlSiCu	AlSiCu
Passivation type	P-VAPOX/NITRIDE/ POLYIMIDE	PSG+Silicon Nitride+Polyimide	Nitride
Assembly information			
Assembly site	ST Bouskoura	ST Bouskoura	ST Bouskoura
Package description	SO8	SO8	SO8
Molding compound	Sumitomo G700KC	EME G700KC	EME G700KC
Frame material	Copper	Cu	Cu
Die attach process	Epoxy Glue	Epoxy Glue	Epoxy Glue
Die attach material	Ablestick 8601 –S25	Ablestick 8601 –S25	8601S-25
Wire bonding process	Tehrmosonic ball bonding	Thermosonic ball bonding	Thermosonic ball bonding
Wires bonding materials/diameters	Cu 1 mil	Cu 1 mil	Cu 1 mil
Lead finishing process	Electroplating	electroplating	electroplating
Lead finishing/bump solder material	Matte Sn	Matte Sn	Matte Sn

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Process/ Package	Product Line	Comments
1	BCD3S/SO8	UW23	Lot CZ5430CN
2	HCMOS4/SO8	16VA	Lot CZ53607S
3	Bipolar/SO8	0393	Lot CZ53005LRP

5.2 Test plan and results summary

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS			Note
						Lot1 UW23	Lot 2 16VA	Lot3 0393	
HTB/ HTOL	N	JESD22 A-108	Ta = 125°C, BIAS		168 H	0/77	0/77	0/78	
					500 H	0/77	0/77	0/78	
					1000 H	0/77	0/77	0/78	
HTSL	N	JESD22 A-103	Ta = 150°C		168 H	0/45	0/45	0/77	
					500 H	0/45	0/45	0/77	
					1000 H	0/45	0/45	0/77	
PC		JESD22 A-113	Drying 24 H @ 125°C JL1 (Store 168 H @ Ta=85°C Rh=85%) JL2 (Store 192 H @ Ta=30°C Rh=60%) Over Reflow @ Tpeak=260°C 3 times		Final	PASS MSLS1	PASS MSLS1	PASS MSLS1	
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121°C		96 H	0/77	0/77	0/77	
					168h	0/77	0/77		
TC	Y	JESD22 A-104	Ta = -65°C to 150°C		200 cy	0/77	0/77	0/77	
					500 cy	0/77	0/77	0/77	
					1000cy		0/77	0/77	
THB	Y	JESD22 A-101	Ta = 85°C, RH = 85%, BIAS		168 H	0/77	0/77		
					500 H	0/77	0/77		
					1000 H	0/77	0/77		

5.3 Tests Description

Test name	Description	Purpose
Die Oriented		
HTOL High Temperature Operating Life **HTB** High Temperature Bias	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTRB High Temperature Reverse Bias **HTFB / HTGB** High Temperature Forward (Gate) Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: low power dissipation; max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
ELFR Early Life Failure Rate	The device is stressed in biased conditions at the max junction temperature.	To evaluate the defects inducing failure in early life.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.

Test name	Description	Purpose
TF / IOL Thermal Fatigue / Intermittent Operating Life	The device is submitted to cycled temperature excursions generated by power cycles (ON/OFF) at T ambient.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
Other		
ESD Electro Static Discharge	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. CBM: Charged Device Model HBM: Human Body Model MM: Machine Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.
LU Latch-Up	The device is submitted to a direct current forced/sunk into the input/output pins. Removing the direct current no change in the supply current must be observed.	To verify the presence of bulk parasitic effect inducing latch-up.